DESIGN PROJECT #1
HALF-ADDER CIRCUIT DESIGN

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ECE 221 Digital Logic Design | Fall 2026 | Dr. Sami Khorbotly
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ABSTRACT

This design procedure will compare how AND, OR, and INVERTER gates can be replicated with NAND and NOR gates, which will prove that they are considered universal gates. With the concept in mind, I have built a half adder using only NOR gates. For these proofs, and the adder, I have designed schematics and created simulated waveforms for these concepts.

♦ INTRODUCTION

The mission of this design project is to prove and verify that NAND and NOR gates are universal gates. A brief overview of what a Universal Gate is: a logic gate that can be used by itself to implement any Boolean function. Initially, circuits were designed to show that NAND gates can in-fact implement the NOT, AND, OR functions. Then, NOR gates are used to implement those same functions. Ultimately, a half adder will be designed only using two-input NOR gates.

♦ PROCEDURE

An outline is given with desired designs listed in *Tutorial A (Found in Canvas)*. Observe circuits produced and timing diagrams in the Appendix.

Part A

I. The following components from the eval library were placed on the schematic:
   a. 7400 two-input NAND gates
   b. 7404 inverter gates
   c. 7408 two-input AND gate
   d. 7432 two-input OR gate

II. NAND gates were connected to produce equivalent inverter, AND, and OR circuits.

III. The input nets were labeled X and Y. The output nets were labeled INV, INV_NAND, AND, AND_NAND, OR, and OR_NAND.

IV. A gate-level simulation profile is made with a run time of 2 µs.

V. The simulation is run, and the corresponding standard-gate and NAND only outputs were compared.

VI. The found implemented circuit expressions are as follows:

i. INV_NAND: (X X)' = X'
ii. AND_NAND: (X' Y')'=X Y
iii. OR_NAND: (X'Y')' =X+Y

Part B

I. The NAND gates are replaced with NOR gates in the circuit.
II. The input nets were labeled X and Y. The outputs were labeled INV, INV_NOR, AND, AND_NOR, OR, and OR_NOR.
III. The existing gate-level simulation profile was used with the same 2 µs run time.
IV. The NOR implementation are:
    i. **INV_NOR: (X+X)' =X'**
    ii. **AND_NOR: (X'+Y')' =XY**
    iii. **OR_NOR: ((X+Y)'+(X+Y)')' = X+Y**

Part C

I. The inputs were labeled X and Y, and the outputs were labeled SUM and COUT.
II. A half-adder was implemented using only two-input NOR gates.
III. The circuit was simulated for 2 µs using gate-level simulation once again.
IV. The output waveforms were checked against the half-adder truth table.
V. For the half-adder:
    i. **SUM = (X+Y)(X'+Y')**
    ii. **COUT = XY**

- **ACKNOWLEDGEMENTS**

The Objectives, Introduction, and Procedure was given and paraphrased from Dr. Sami Khorbotly in his design handout as per linked in the Procedure section.

APPENDIX

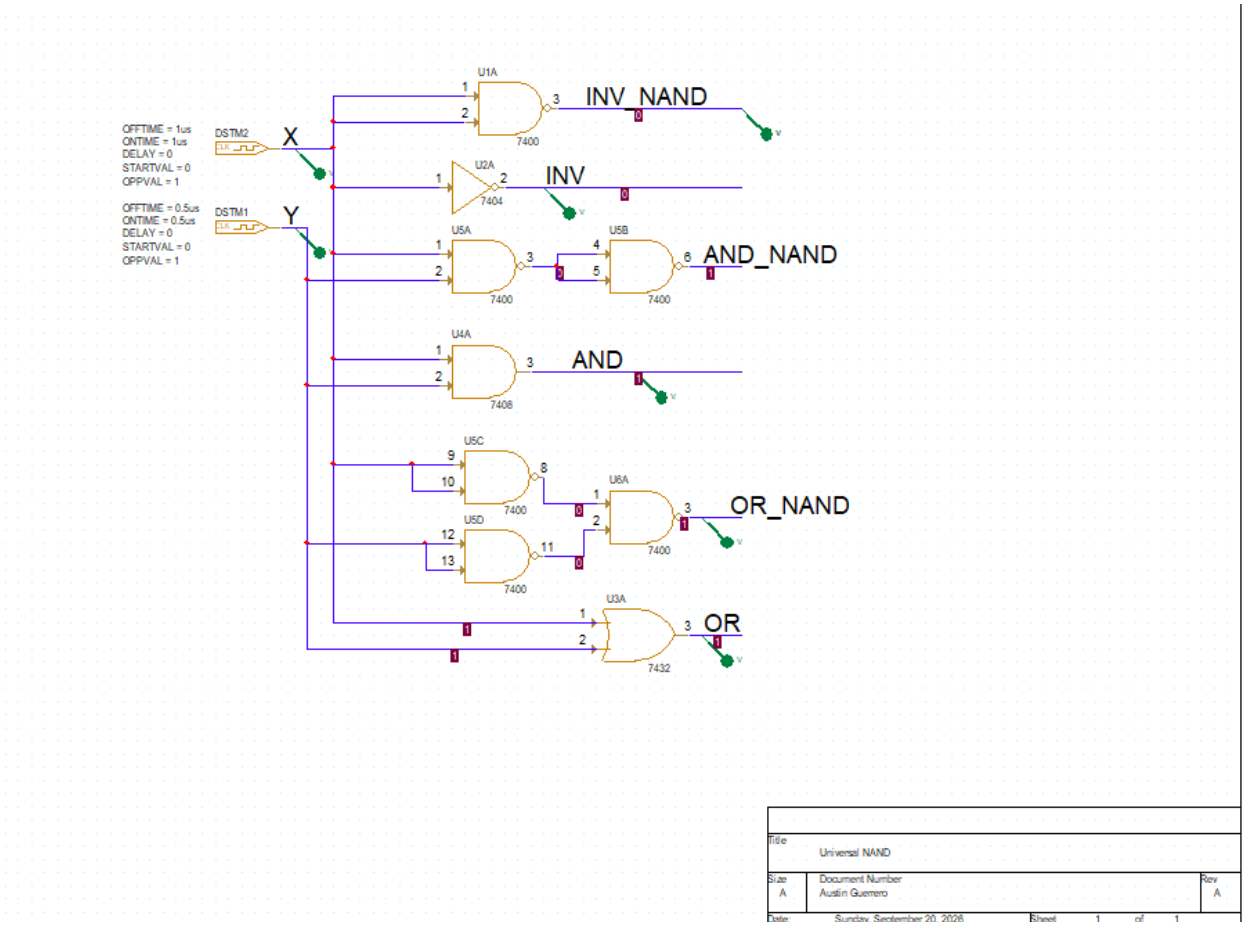


Fig 1. ***(Universal NAND schematic)***

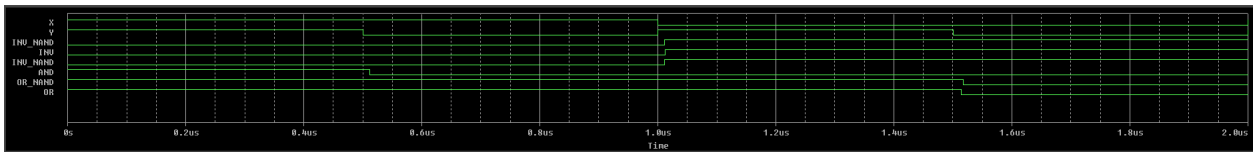


Fig 2. ***Full Timing Diagram of AND – OR – NOT Circuits implemented with NAND***

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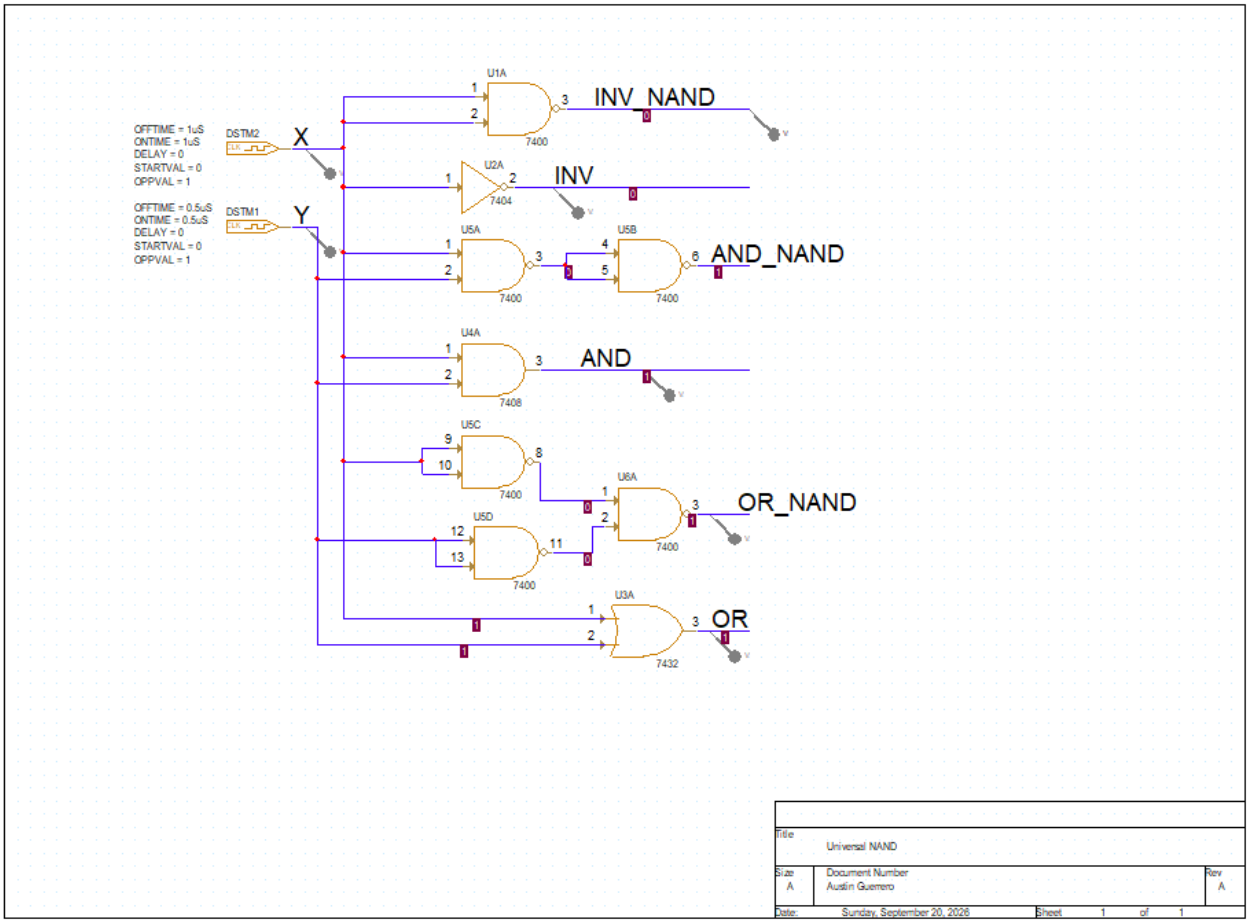


Fig 3. Universal NOR schematic

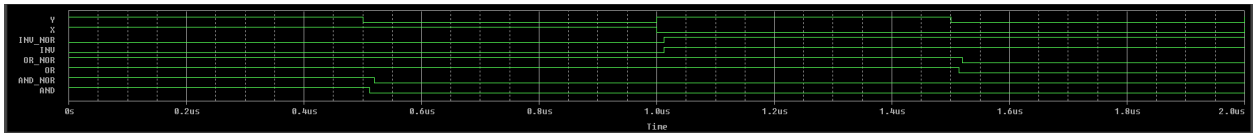


Fig 4. ***Full Timing Diagram of AND – OR – NOT Circuits implemented with NOR***

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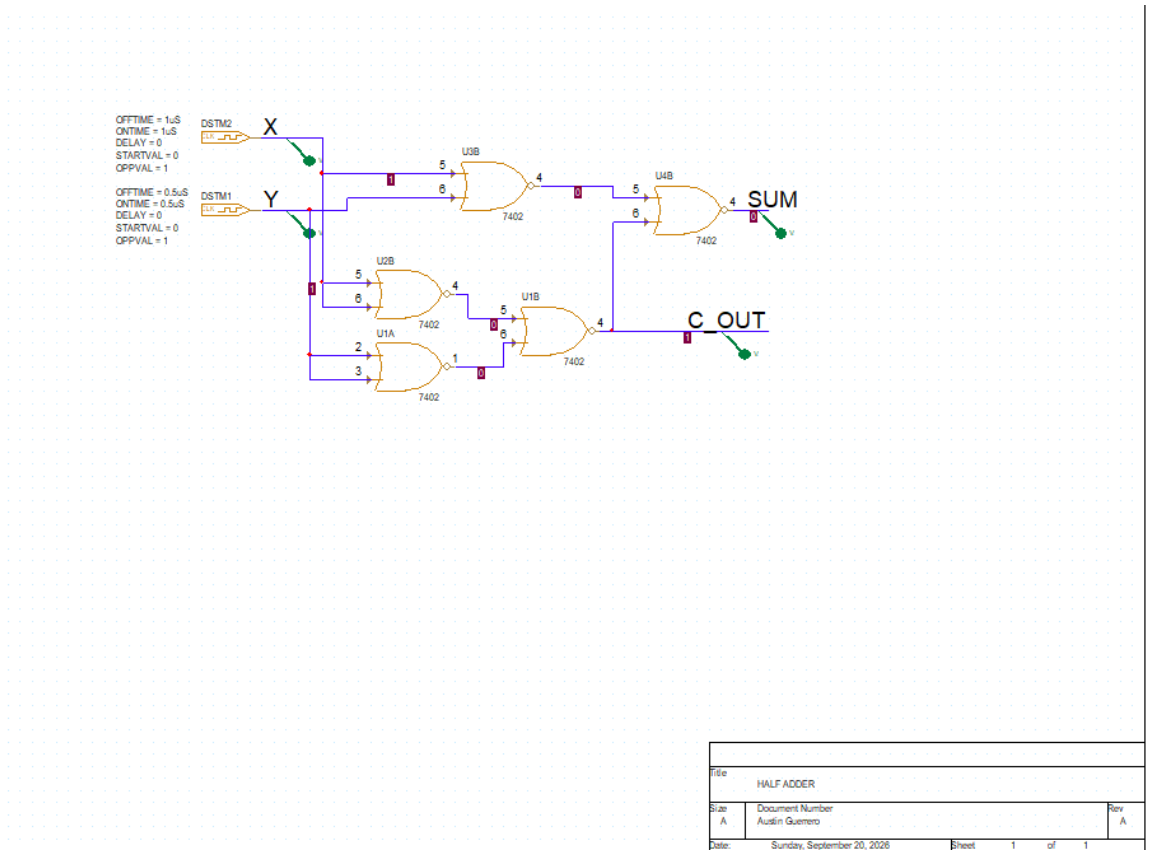


Fig 5. ***Half-Adder Circuit Diagram***

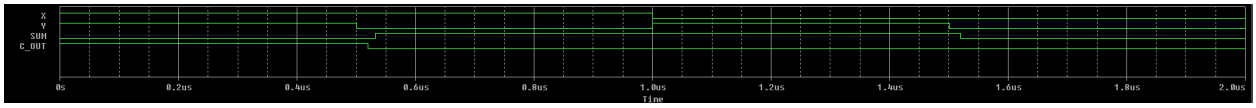


Fig 6. ***Half-Adder Waveform Diagram***

APPENDIX

Valparaiso University
Department of Electrical and Computer Engineering
ECE 221: Digital Logic Design

Design Project #1: Universal Gates

Name: Austin Guerrero

1. NOR functions:

$f_{NOR}(X, X) =$ $\overline{X + X}$ $= \bar{X} = f_{INV}(X)$

$f_{NOR}(\bar{X}, \bar{Y}) =$ $\overline{X' + Y'}$ $= X \cdot Y = f_{AND}(X, Y)$

$f_{NOR}(X, Y) =$ $\overline{X + Y}$ $= X + Y = f_{OR}(X, Y)$

2. Completed truth table for the Half Adder.

X	Y	SUM	COUT
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

3. Minimized boolean expressions in POS form for the half adder.

SUM = $(x+y)(\bar{x}+\bar{y})$

COUT = xy

Honor Code Pledge:

"I have neither given or received, nor have I tolerated others' use of unauthorized aid."

Signature: Austin Guerrero

9

Fig 7. ***Lab Cover with Theory Analysis***